What Is Claimed Is:

1. Byte alignment circuitry comprising:

a data input;

a control input;

a special character selection input indicating which special character is to be used for byte alignment; and

a special character status output indicating which special character was used to align the byte boundaries; and

a data output.

2. The circuitry defined in claim 1 wherein said data input is one of a plurality of parallel data inputs.

3. The circuitry defined in claim 2 wherein said plurality is the number of bits in a byte.

4. The circuitry defined in claim 1 wherein said data output is one of a plurality of parallel data outputs.

5. The circuitry defined in claim 4 wherein said plurality is the number of bits in a byte.

6. The circuitry defined in claim 5 wherein successive aligned bytes are output one after another via the data outputs.

7. The circuitry defined in claim 1 further comprising a clock input.

8. A digital processing system comprising:

processing circuitry;

a memory coupled to the processing circuitry; and

byte alignment circuitry as defined in claim 1 coupled to said processing circuitry and said memory.

9. A printed circuit board on which is mounted byte alignment circuitry as defined in claim 1.

10. The printed circuit board defined in claim 9 further comprising:

a memory mounted on said printed circuit board and coupled to said byte alignment circuitry.

11. The printed circuit board defined in claim 9 further comprising:

processing circuitry mounted on said printed circuit board and coupled to said byte alignment circuitry.

12. Circuitry for receiving and byte-aligning data comprising:

byte alignment circuitry that uses a first special character selected by a special character selection signal to detect byte boundaries in received data, and aligns the byte boundaries when enabled by a control signal to subsequently output byte-aligned data and a special character status signal indicative of the special character used to align the byte boundaries; and

utilization circuitry responsive to outputs of the byte alignment circuitry and selectively providing said control signal and said special character selection signal.

13. The circuitry defined in claim 12 wherein the byte-aligned data is output in parallel form.

14. The circuitry defined in claim 12 wherein said utilization circuitry comprises programmable logic circuitry.

15. The circuitry defined in claim 12, wherein said byte alignment circuitry outputs a pattern detect signal indicative of the presence of byte aligned data; and

said pattern detect signal causes said utilization circuitry to disable said control signal.

16. The circuitry defined in claim 12, wherein said byte alignment circuitry automatically prevents alignment to subsequently received data containing byte boundary data after the byte boundaries have already been aligned.

17. The circuitry defined in claim 12, wherein said byte alignment circuitry provides data representing said first special character to said utilization circuitry.

18. The circuitry defined in claim 12, wherein said special character select signal can instruct said byte alignment circuitry to use a second special character to detect the byte boundaries in received data.

19. The circuitry defined claim 18, wherein said byte alignment circuitry re-aligns the byte

boundaries using said second special character when enabled by said control signal.

20. Circuitry for receiving and byte-aligning data comprising:

byte alignment circuitry that processes received data and outputs byte-aligned data after byte boundaries are aligned, said byte alignment circuitry further comprising:

special character detection circuitry that detects a selected special character in the received data, said selected special character is selected based on a selection signal; and

boundary adjustor circuitry that sets the byte boundaries when said selected special character is detected and criteria are met; and

utilization circuitry that receives the outputs of said byte alignment circuitry.

21. The circuitry defined in claim 20, wherein said selection signal is hardwired to permanently select a particular selected special character.

22. The circuitry defined in claim 20, wherein said utilization circuitry provides said selection signal to select a particular special character.

23. The circuitry defined in claim 20, wherein said byte alignment circuitry disables said boundary adjustor circuitry independent of a control signal.

24. The circuitry defined in claim 20, wherein said utilization circuitry enables said boundary adjustor circuitry by providing a control signal to said byte alignment circuitry.

25. The circuitry defined in claim 20, wherein said byte alignment circuitry further comprising constructor circuitry.